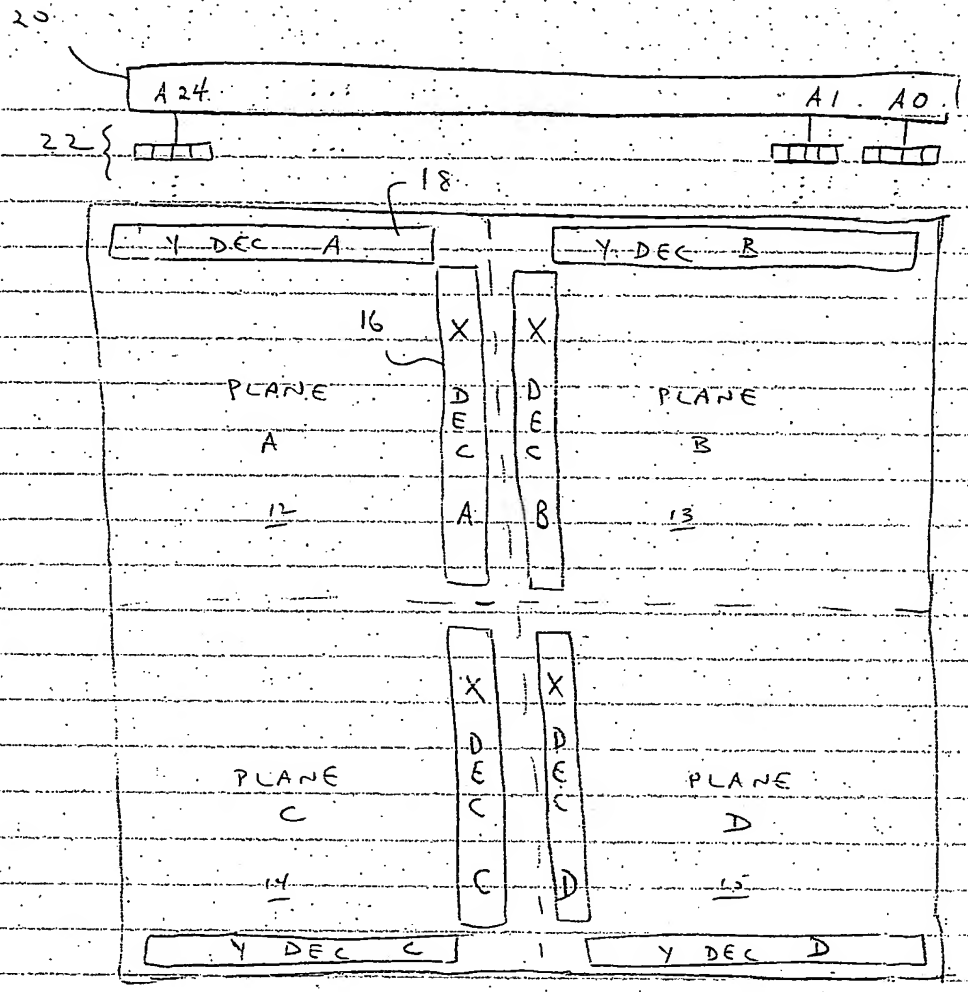
20
A24
A1
A0
10
22
18
Y DEC A
Y DEC B
16
X
DEC
A
B
PLANE
A
B
12
13
C
D
14
15
Y DEC C
Y DEC D

FIG 1

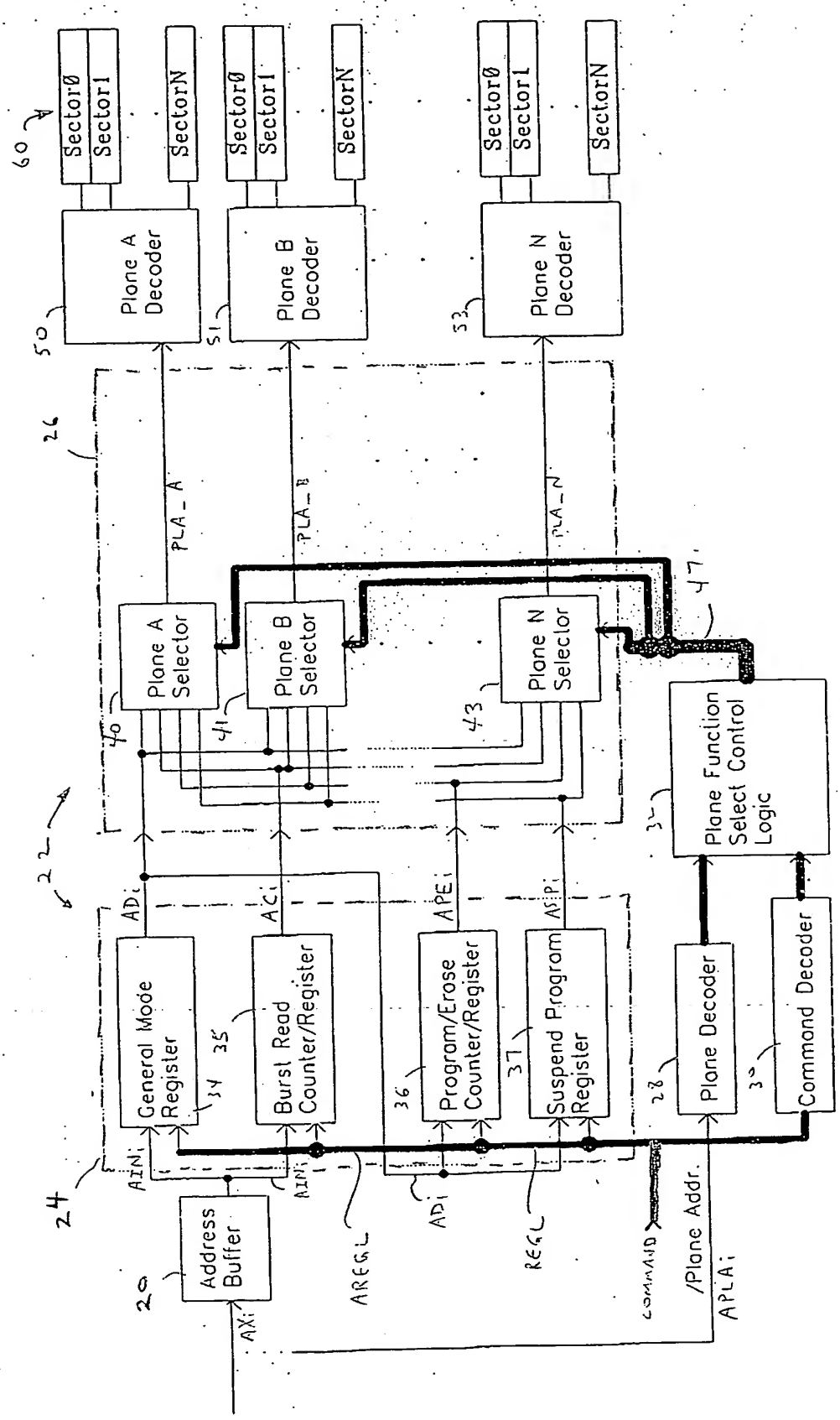
Sector0
Sector1
SectorN
Plane A Decoder
Plane B Decoder
Plane N Decoder
PLA_A
PLA_B
PLA_N
Plane A Selector
Plane B Selector
Plane N Selector
Plane Function Select Control Logic
General Mode Register
Burst Read Counter/Register
Program/Erase Counter/Register
Suspend Program Register
Plane Decoder
Command Decoder
Address Buffer
AREGL
ADi
REGL
COMMAND
/Plane Addr.
APLAi
AXi
AINi
ADi
ACi
APEi
APPi
60
50
51
53
26
22
24
20
40
41
43
47
34
35
36
37
28
38
32

Fig. 2

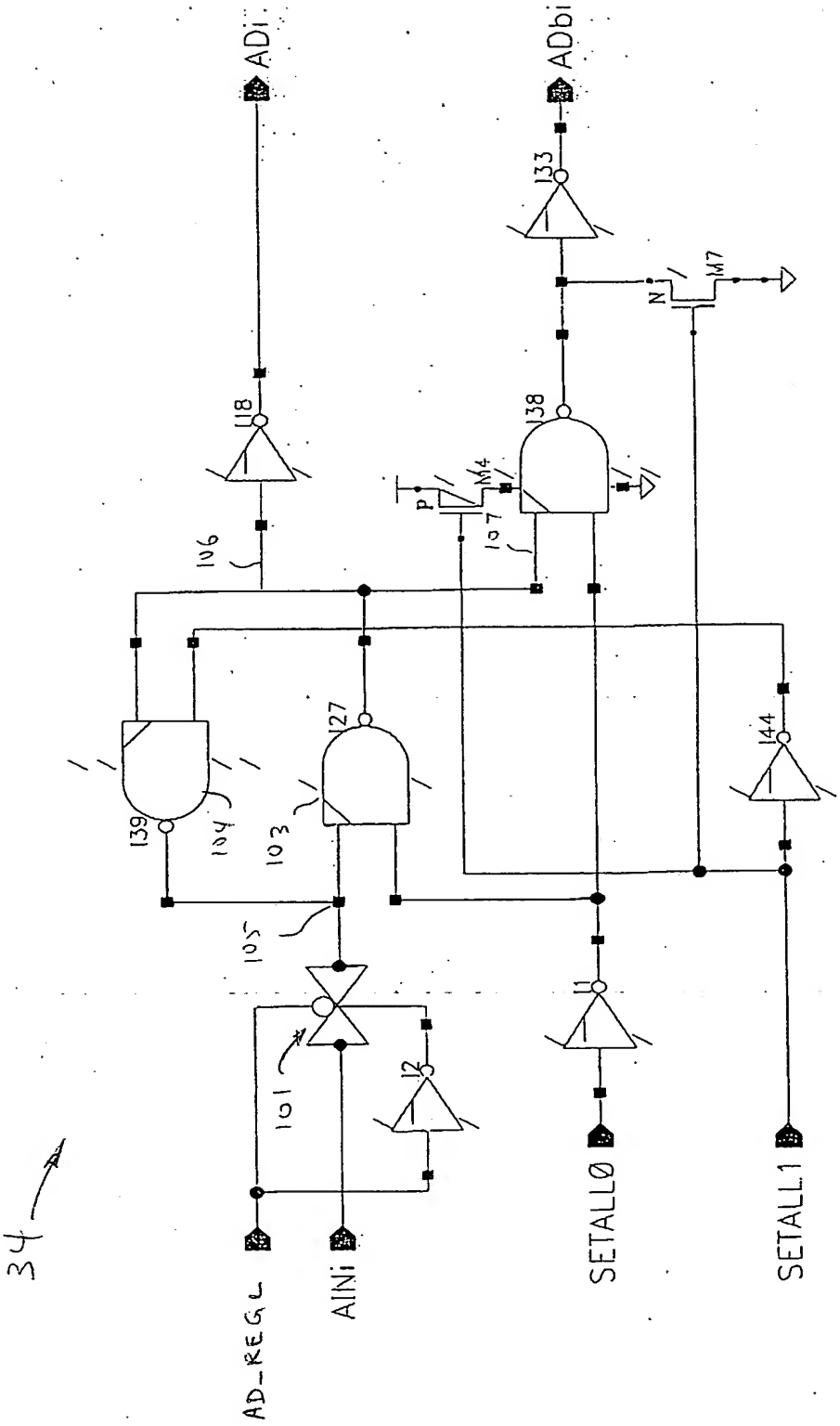
ADi
ADbi
133
M7
N
118
138
M4
P
107
106
127
144
139
104
103
105
101
12
11
AD_REGL
AINi
SETALLØ
SETALL1
34

Fig. 3

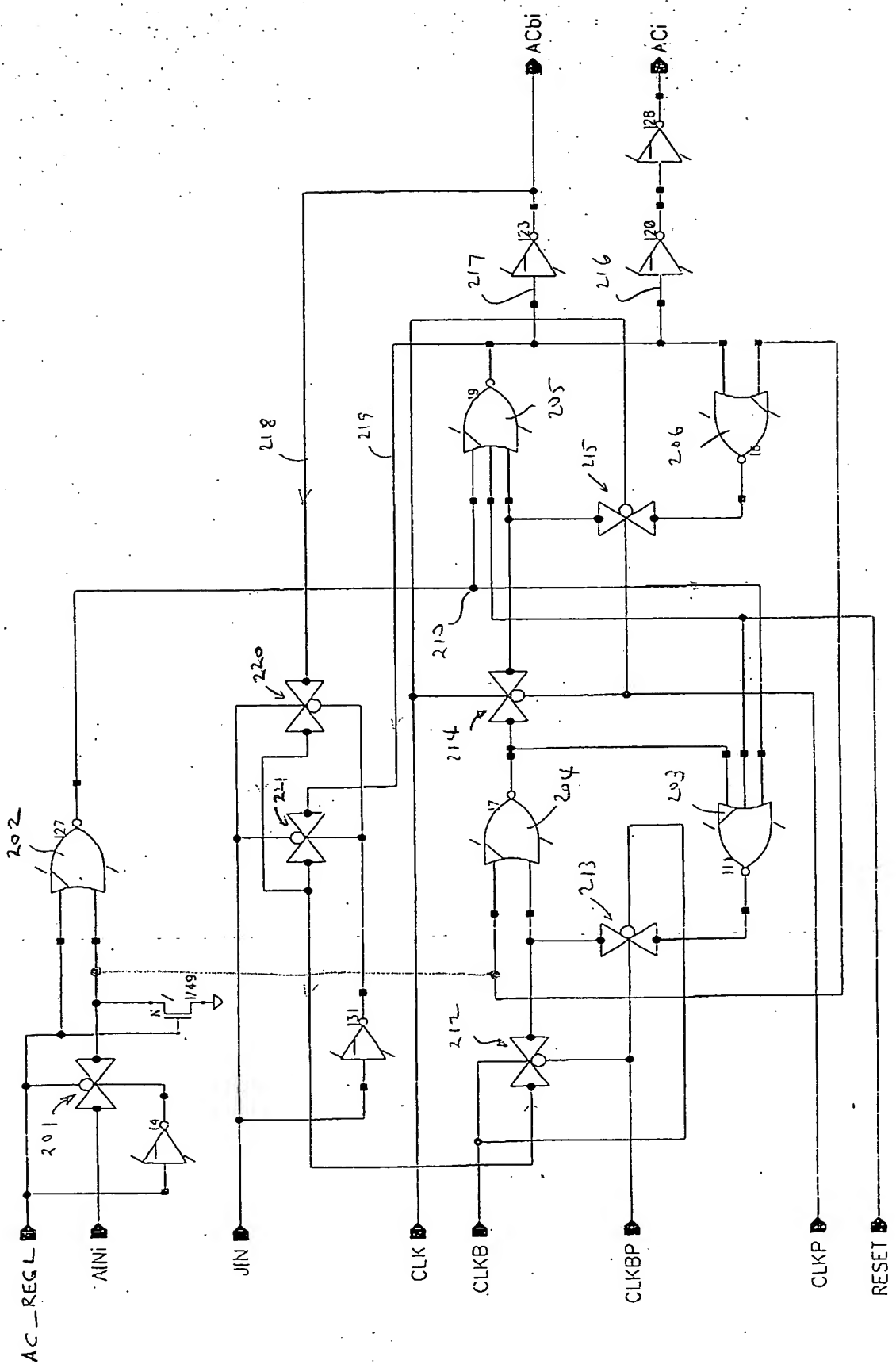
ACbi
ACi
AC_REGL
AINi
JIN
CLK
CLKB
CLKBP
CLKP
RESET
35
201
202
204
206
211
212
213
214
215
216
217
218
219
220
221
231
235

Fig. 4

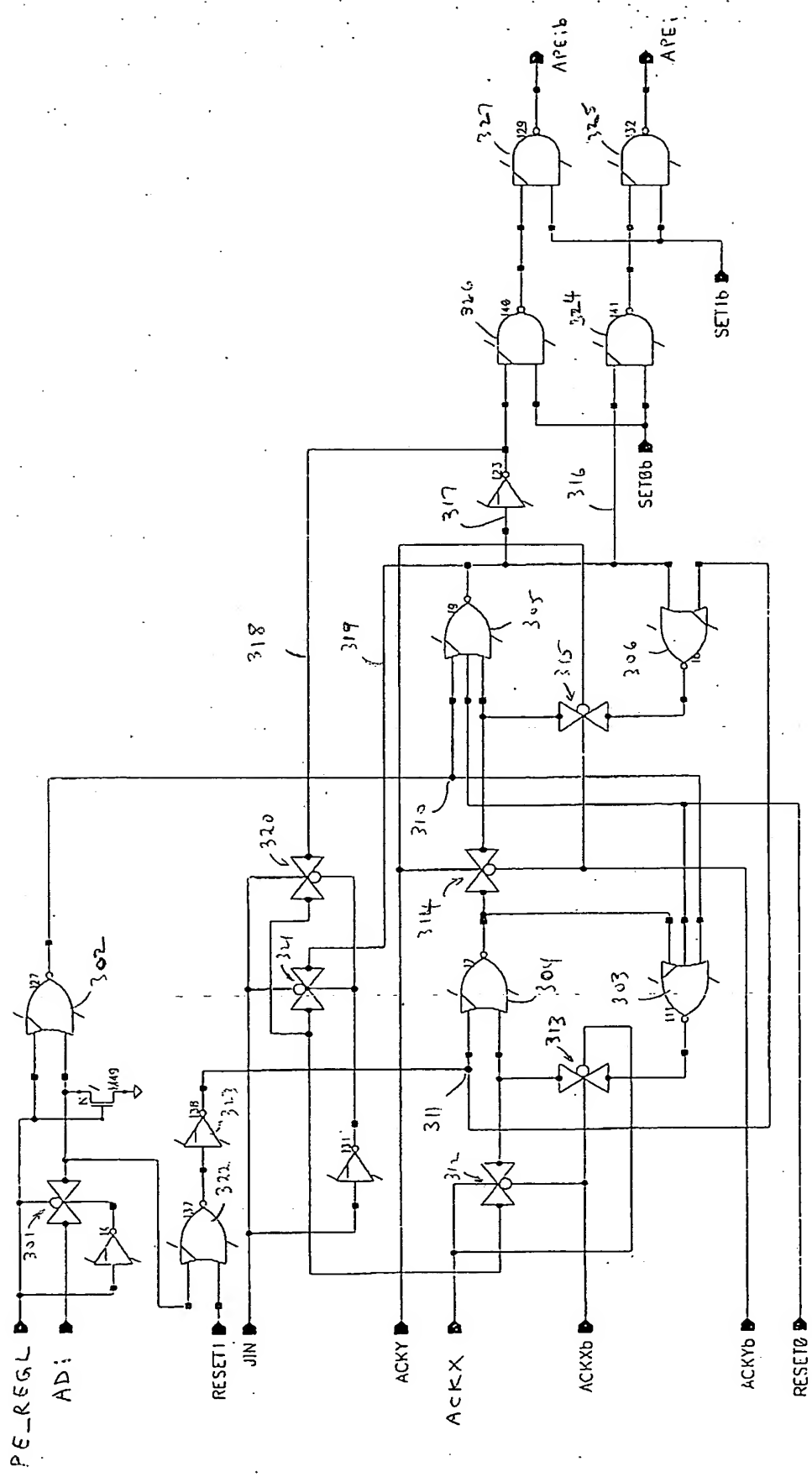
PE_REGL
ADi
RESETi
JIN
ACKY
ACKX
ACKXb
ACKYb
RESETb
SETib
SETOb
APEib
APEi
302
303
304
305
306
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327

Fig. 5

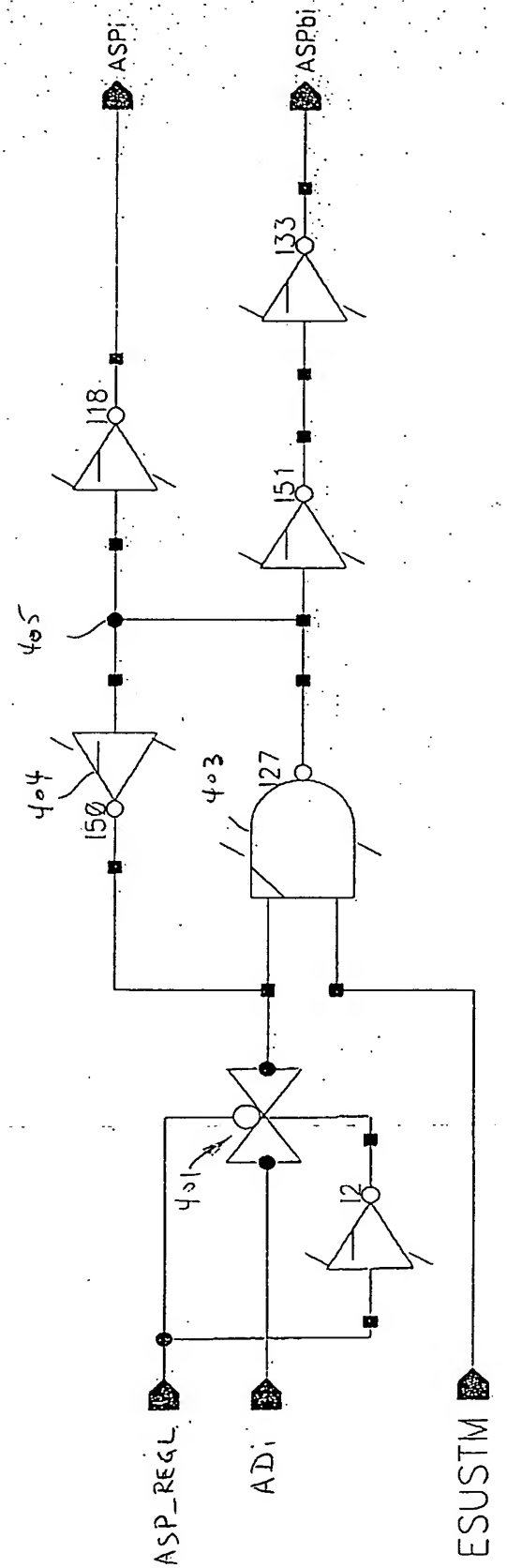
ASPi
ASPbi
133
118
151
405
404
150
403
127
431
12
ASP_REGL
ADi
ESUSTM

Fig. 6

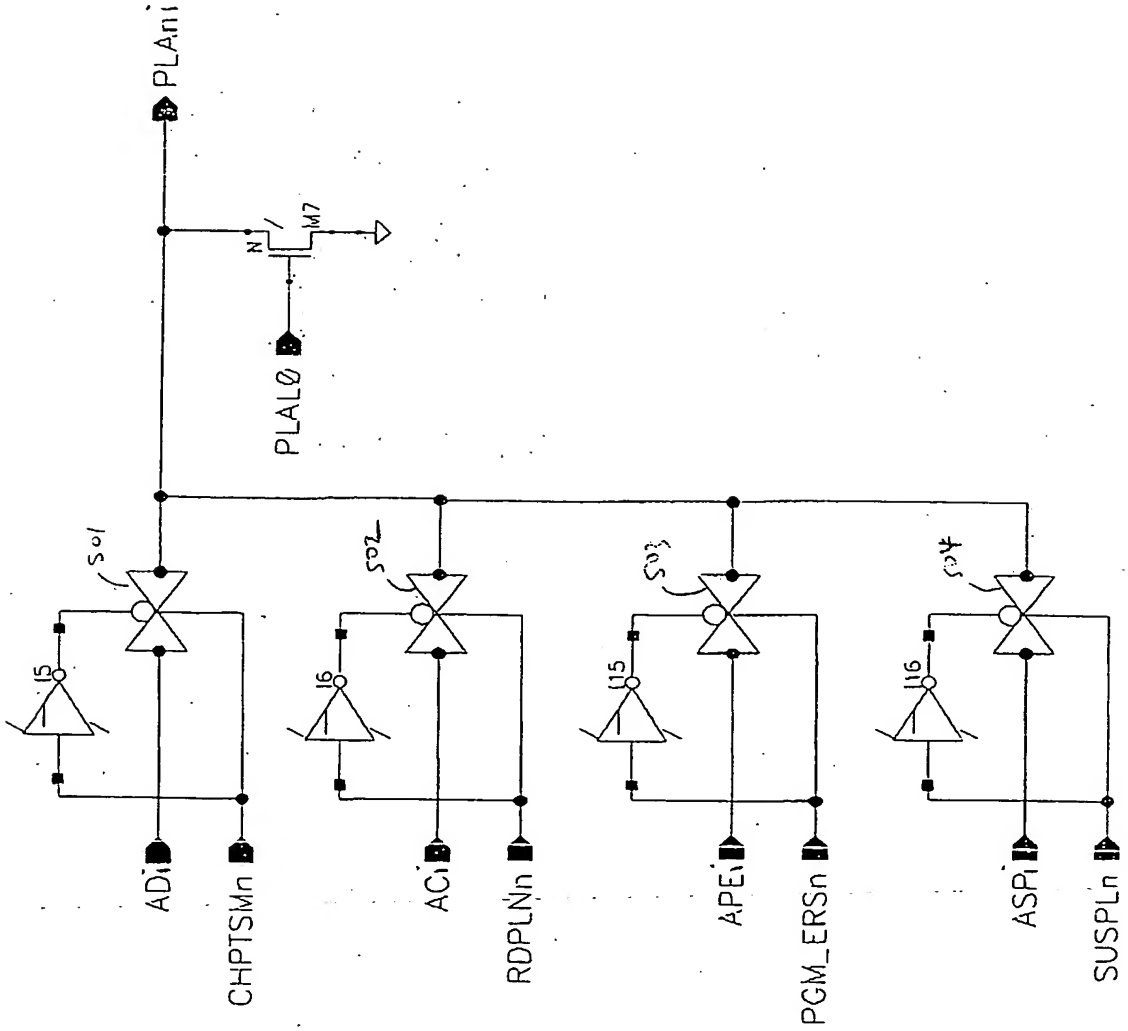
PLAni
M7
N
PLAL0
S01
S02
S03
S04
I5
I6
I15
I16
ADi
CHPTSMn
ACi
RDPLNn
APEi
PGM_ERSn
ASPi
SUSPLn

Fig. 7